Remarks

This preceding amendments and following remarks are provided in response to the Official Action of the Examiner mailed February 13, 2003, setting a three-month shortened statutory period for response ending May 13, 2003. Claims 1-3, 5, 7-12 and 14-65 remain pending. Claims 1, 5, 7, 12, 14-15, 24-26 and 33 have been amended, claims 58-65 have been added, and claims 4, 6 and 13 have been canceled without prejudice.

On page 2 of the Office Action, the Examiner rejected claims 1-8, 12-21 and 24-31 under 35 U.S.C. § 102(b) as being anticipated by Noddings et al. (U.S. Patent No. 5,574,814). With respect to claim 1, the Examiner states that Noddings suggest a window (citing Fig. 2; column 3, lines 60-61), a chip fixed on a first side of said window (citing column 4, lines 1-3), and a first housing extending around said chip and fixed relative to said window (citing Fig. 2).

In response, Applicant has amended claim 1 to recite:

1. (Amended) A chip-scale package for photonic devices, comprising:
a window having one or more conductive traces on a first side of said window;
a chip fixed ~~on a~~ relative to the first side of said window; ~~and~~
a first housing extending around said chip and fixed relative to said window;
said chip having one or more electrical terminals;
said first housing having one or more electrical terminals; and
at least one terminal of said chip being bump bonded to a conductive trace on said window, and at least one terminal of said first housing being bump bonded to a conductive trace on said window.

As can be seen, claim 1 now recites that at least one terminal of said chip is bump bonded to a conductive trace on said window, and at least one terminal of said first housing is bump bonded to a conductive trace on said window. Claims 4 and 6 have been canceled without prejudice.

With respect to claims 4 and 6, the Examiner cites to column 5, lines 2-7 of Noddings et al. which states:

> Flex 116 can also be connected to metalized circuit traces within sapphire window 114 instead of directly to VCSEL 115. This connection from VCSEL 115 to flex 116 can be made by wire bond/flipchip/TAB connections from VCSEL 115 to the metalized traces on sapphire window 114.

As can be seen, this merely suggests connecting flex 116 to metalized circuit traces within the sapphire window, and connecting VCSEL 115 to the metalized traces using wire bond/flipchip/ TAB connections. Nowhere does Nodding et al. suggest bump bonding at least one terminal of said chip to a conductive trace on said window, and bump bonding at least one terminal of said first housing to a conductive trace on said window. In fact, it is not clear why, for example, bump bonding would be used to bond flex 116 to the metalized traces within the sapphire window. Noddings certainly does not suggest this. In view of the foregoing, claim 1 is believed to be clearly patentable over Noddings et al. For similar and other reasons, dependent claims 2-3, 5, 7-11 are also believed to be clearly patentable over Noddings et al.

Now turning to claim 12. Claim 12 has been amended to recite:

> 12. (Amended) A chip-scale package for photonic devices, comprising:
> a first housing <u>having an electrically conductive internal pad</u>;
> a chip attached relative to said first housing, <u>the chip having an electrically conductive pad that faces the window</u>; and
> a window attached relative to said first housing, <u>wherein the internal pad of the housing faces said window;</u>
> <u>at least one conductive trace formed on said window; and</u>
> <u>wherein the at least one conductive trace is electrically connected to the pad of said chip and to the internal pad of said first housing</u>.

As can be seen, claim 12 now recites a first housing that has an electrically conductive internal pad that faces the window, a chip that has an electrically conductive pad that faces the window,

and at least one conductive trace formed on said window. Claim 12 further recites that the at least one conductive trace is electrically connected to the pad of said chip and to the internal pad of said first housing.

Nodding et al. clearly does not suggest a housing that includes an electrically conductive internal pad that faces the window, and more specifically, an electrically conductive internal pad that faces the window which is electrically connected to a conductive trace that is formed on the window. Instead, it appears that Nodding et al. suggest using Flex 116, which appears to be a bundle of wires. Nodding et al. state:

> Flex 116 provides a compliant alignment between active optical components, such as VCSEL 115 and fibers 103. Furthermore, the use of flex 116 for the interface between substrate 129 and VCSEL 115 allows for a 90 orientational difference in order to redirect surface sensitive optical components from the horizontal to the vertical.

(Noddings et al., column 4, line 64 through column 5, line 2). In view of the foregoing, claim 12 is believed to be clearly patentable over Noddings et al. For similar and other reasons, dependent claims 14-23 are also believed to be clearly patentable over Noddings et al.

Now turning to claim 24. Claim 24 has been amended to recite:

> 24. (Amended) A hermetic chip-scale package comprising:
> a first housing;
> an integrated circuit mounted within said first housing, the integrated circuit having at least one terminal;
> a window secured relative to said first housing; and
> wherein:
> said integrated circuit has at least one photonic device; and
> said first housing and said window form a hermetically sealed enclosure around said integrated circuit, said housing having a body with at least one conductor extending through said body from the hermitically sealed enclosure to external to the hermitically sealed enclosure, the at least one conductor having a low resistance path to a terminal of the integrated circuit.

As can be seen, claim 24 now recites that the housing includes a body with at least one conductor extending through said body from the hermitically sealed enclosure to external to the hermitically sealed enclosure. Claim 24 further recites that the at least one conductor has a low resistance path to a terminal of the integrated circuit. Flex 116 of Noddings et al. does not extend through the body of the housing from the hermitically sealed enclosure to external to the hermitically sealed enclosure. Instead, flex 116 of Noddings et al. appear to be always within the sealed enclosure of the housing.

In addition, flex 116 of Noddings et al. appears to provide a connection from VCSEL 115 to circuit block 131. With respect to circuit block 131, Noddings et al. state:

> The electrical signals to VCSEL 115 are manipulated, driven and received by circuitry within circuit block 131. Circuit block 131 may contain well-known circuit components, such as resistors, capacitors, and drivers commonly used within such an assembly. Circuit block 131 may be monolithic or discrete in design. Circuit block 131 is encased by substrate 129, seal ring 132, lid 128 and seal plate 123. External electrical access to the circuits within circuit block 131 is provided by wire assembly 130.

(Noddings et al., column 4, lines 27-34). Thus, external electrical access is provided by wire assembly 130, and not flex 116. However, wire assembly 130 does not appear to provide a low resistance path to a terminal VCSEL 115. Instead, wire assembly 130 appears to provide a low resistance path to circuit block 131. In view of the foregoing, claim 24 is believed to be clearly patentable over Noddings et al. For similar and other reasons, dependent claims 25-32 are also believed to be clearly patentable over Noddings et al.

Now turning to claim 33. Claim 33 recites:

> 33. (Amended) A chip-scale package for electronic devices, comprising:
>
> a transparent window having at least one conductive trace patterned on a surface of said window;

a semiconductor chip fixed relative to said window having at least one terminal connected to the at least one conductive trace;
a first housing surrounding said chip and affixed to said window; and
a conductive path from the at least one conductive trace to an at least one pad on an external surface of said enclosure.

As can be seen, claim 33 recites a semiconductor chip fixed relative to said window having at least one terminal connected to the at least one conductive trace, and a conductive path from the at least one conductive trace to at least one pad on an external surface of said enclosure. At the bottom of page 5 of the Office Action, the Examiner acknowledges that Noddings et al. do not teach providing a conductive path from the at least one conductive trace to an at least one pad on an external surface of said enclosure, as claimed. However, the Examiner states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to include this because it is notoriously well known (NWK) for traces to perform such a function in such applications.

After careful review, Applicant must respectfully disagree. First, it appears that Noddings et al. would actually teach away from providing a conductive path from the at least one conductive trace to at least one pad on an external surface of said enclosure. Noddings et al. suggest providing Flex 116, which can be connected to metalized circuit traces within sapphire window 114 (Noddings et al., column 5, lines 2-4). According to Noddings et al., an advantage of this is that:

> Flex 116 provides a compliant alignment between active optical components, such as VCSEL 115 and fibers 103. Furthermore, the use of flex 116 for the interface between substrate 129 and VCSEL 115 allows for a 90 orientational difference in order to redirect surface sensitive optical components from the horizontal to the vertical.

(Noddings et al., column 4, line 64 through column 5, line 2).

In addition, Flex 116 of Noddings et al. does not provide a conductive path from the at least one conductive trace to an at least one pad on an external surface of said enclosure. Instead, flex 116 is always within the sealed enclosure of the housing, and appears to provide a connection from VCSEL 115 to circuit block 131. With respect to circuit block 131, Noddings et al. state:

> The electrical signals to VCSEL 115 are manipulated, driven and received by circuitry within circuit block 131. Circuit block 131 may contain well-known circuit components, such as resistors, capacitors, and drivers commonly used within such an assembly. Circuit block 131 may be monolithic or discrete in design. Circuit block 131 is encased by substrate 129, seal ring 132, lid 128 and seal plate 123. External electrical access to the circuits within circuit block 131 is provided by wire assembly 130.

(Noddings et al., column 4, lines 27-34). Thus, external electrical access is provided by wire assembly 130, and not flex 116. As such, it is unclear why it would have been obvious to include a conductive path from the at least one conductive trace patterned on the window to an at least one pad on an external surface of said enclosure, as claimed, even if it is NWK for traces generally to perform such functions in some applications.

In any event, Applicant does not believe it is NWK to provide a conduction path from the at least one conductive trace that is patterned on a window to an at least one pad on an external surface of said enclosure, as recited in claim 33. As noted in the MPEP, the Examiner should not be obliged to spend time to produce documentary proof for that which is well known. However, if the applicant traverses such an assertion, the Examiner should cite a reference in support of his or her position. Applicant hereby traverses the Examiner assertion that it is NWK to provide a conduction path from the at least one conductive trace that is patterned on a window to an at least one pad on an external surface of said enclosure, as recited in claim 33. As such, Applicant respectfully requests that the Examiner provide documentary proof of such assertion.

In view of the foregoing, claim 33 is believed to be clearly patentable over Noddings et al. For similar and other reasons, dependent claims 34-57 are also believed to be clearly patentable over Noddings et al.

Applicant has added newly presented claims 58-65. Newly presented claim 58-61 are either directly or indirectly dependent from claim 1. Thus, for reasons similar to those given above with respect to claim 1, as well as other reasons, newly presented claims 58-61 are believed to be clearly patentable over Noddings et al. Newly presented claims 62-65 are also believed to be clearly patentable over Noddings et al.

In view of the foregoing, Applicant believes that all pending claims 1-3, 5, 7-12 and 14-65 are now in condition for allowance. Examination and reconsideration are respectfully requested. If a telephone conference might be of assistance, please contact the undersigned attorney at (612) 677-9050.

Respectfully submitted,

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By His Attorney,

Dated: May 12, 2003

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